Photonic Switching Architectures with Logic Cells

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ABSTRACT

Possible switching architectures, with Optically Programmable Logic Cells - OPLCs - will be reported in this paper. These basic units, previously employed by us for some other applications mainly in optical computing, will be employed as main elements to switch optical communications signals. The main aspect to be considered is that because the internal components of these cells have nonlinear behaviors, namely either pure bistable or SEED-like properties, several are the possibilities to be obtained. Moreover, because their properties are dependent, under certain condition, of the signal wavelength, they are apt to be employed in WDM systems and the final result will depend on the corresponding optical signal frequency.

We will give special emphasis to the case where self-routing is achieved, namely to structures of the Batcher or Banyan type. In these cases, as it will be shown, there is the possibility to route any packet input to a certain direction according to its first bits. The number of possible outputs gives the number of bits needed to route signals.

An advantage of this configuration is that a very versatile behavior may be allowed. The main one is the possibility to obtain configurations with different kinds of behavior, namely, Strictly Nonblocking, Wide-Sense Nonblocking or Rearrangeably Nonblocking as well as to eliminate switching conflicts at a certain intermediate stages.

Keywords: Photonic switching, Optical computing, WDM.

1. INTRODUCTION

Most of the published works concerning optical bistable devices have been related with some type of optical computing. In the beginning of the eighties, when this effect was initially analyzed, the main objective was obtaining devices with two principal characteristics, namely, high switching speed and low level of power consuming. These objectives were partially obtained but their application to optical computers seemed a very distant goal. The reason was that the potential obtained advantages were insufficient when compared with the results achieved by their electronic counterparts. Although the theoretical maximum switching speed is much higher than the obtained by conventional processors, the complexity of optical architectures makes them very difficult for develop an all-optical computer. A point should be indicated concerning this difficulty. One of the main lines followed to establish the general frame for an optical computer was to develop architectures similar to those employed in electronic computers. This means that most of the processes follow a serial configuration. This philosophy, obvious when employed signals are electrical, is not so obvious when are optical the signals to be used. One of the more important properties of light is its inherent capability to work in a parallel way. This property is the basis for common image processors employing devices as, for example, spatial light modulators.

Although the application of optical bistable devices to optical computing was not so brilliant as fist proposals indicated some years before, their use in other fields, mainly optical communications, kept them in a priority level. In this way, configurations to be employed in photonic switching may employ different types of optical bistability to perform tasks as signals routing and packet switching. Hence, optical computing has been a very useful tool to develop structures able to work in optical communications.

The introduction of photonic switching with optical bistability concepts has been, in this way, one of the possible improvements in future optical communications systems. This fact came together with other very important concept developed in the last years too. This concept is wavelength division multiplexing, WDM. A single fiber is now employed to carry several channels with different wavelengths and they go though the same way without any type of

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Optical Transmission Systems and Equipment for WDM Networking II, Benjamin B. Dingel, Werner Weiershausen, Achyut K. Dutta, Ken-Ichi Sato, Editors, Proceedings of SPIE
Vol. 5247 (2003) © 2003 SPIE · 0277-786X/03/$15.00

mutual interference or crosstalk. Different signals going through the same physical space may perform different type of operations. Although it is the same space, this characteristic may be related with the parallel properties of light. As a matter of fact, it is possible to call this characteristic as a type of space multiplexing.

A new possible further step in this process may now be proposed. Most of the nowadays switching and routing configurations employ passive structures to process different lambda signals. They are based on several types of structures, for example, Bragg gratings and different types of etalons. In the first case, a demultiplexed signal, with different lambdas going through different paths, is obtained. In the second one, optical frequencies in a certain band are blocked and other frequencies go out of the structure. Almost in any case, operation is passive in the sense that a particular configuration gives rise to a particular result. A possible way to improve this behavior should be to apply concepts employed in optical computing, in general, and in programmable logic, in particular, to introduce a type of active behavior.

Moreover, another way to approach to optical computing it is possible too. As it has been pointed out before, one of the main drawbacks in optical computing is the serial character of most of the employed configurations. The parallel properties of light are not present in any one of the reported architectures. The present WDM systems in optical communication allow a possible way to implement a certain type of parallel processing. Different signals to be processed at a certain time may go together through an optical fiber in a parallel way. It will be necessary just to separate them at a certain point and perform the desired operation. Signals may no go, as customary, in a serial form. This possibility opens a different form to operate. As it will be shown in this paper, some possibilities may derive from the above indicated possibility.

From these considerations, a new possible form to work in optical communications and in optical computing will be reported in this paper. We will try first to establish some general concepts, most of them based on previous theories. We will develop some principles in order to develop those concepts. Some of these principles have been employed by the authors in previous works. This paper will present a general framework to handle conventional packets with concepts employed in optical computing, namely, logic cell. As a consequence of those ideas, a particular example will be reported concerning routing packets in conventional switching structures.

2. PANORAMIC VIEW OF SOME SWITCHING NETWORKS

The concept of self-routing is attractive in packet switching where routing is performed at each switching stage according to the destination address of an input packet. In this case must be an address decoding logic at each crosspoint. From this arrangement, a separate switching control to configure the switching fabric is unnecessary. In practice, an input packet carries its routing information through either its virtual circuit identifier (in virtual circuit) or its destination node address (in datagram). When the packet is routed through the switch, one bit at a time of its p-bit address is used for switching at a stage. Although a general theory about photonic switching may be seen in any textbook[1], we will present here some basic concepts in order to synthesize the main concepts to be implemented later.

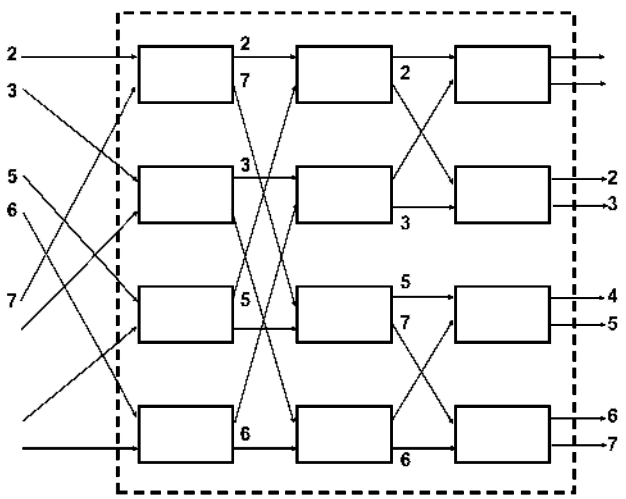

Fig. 1.- A simplified 8 x 8 Banyan network.

A Banyan routing network is shown in Fig. 1. If (m_1, m_2, m_3) is the triple binary output port address of an incoming packet, bit m_i will be used for routing at stage i. Otherwise, it will be routed to the upper port. For example, if an incoming packet at input port 3 has an output address 6 (both in the range from 0 to 7) or (110), it will be routed down in the first stage, stay down in the second stage,

and then go up in the last stage. A possible problem appears if, for example, another incoming packet at input port 2 that has an output port address 5 (101), it needs to be routed down at the same first stage switch than the previous packet. Therefore, there is a switching conflict, or an internal blocking, at the first stage.

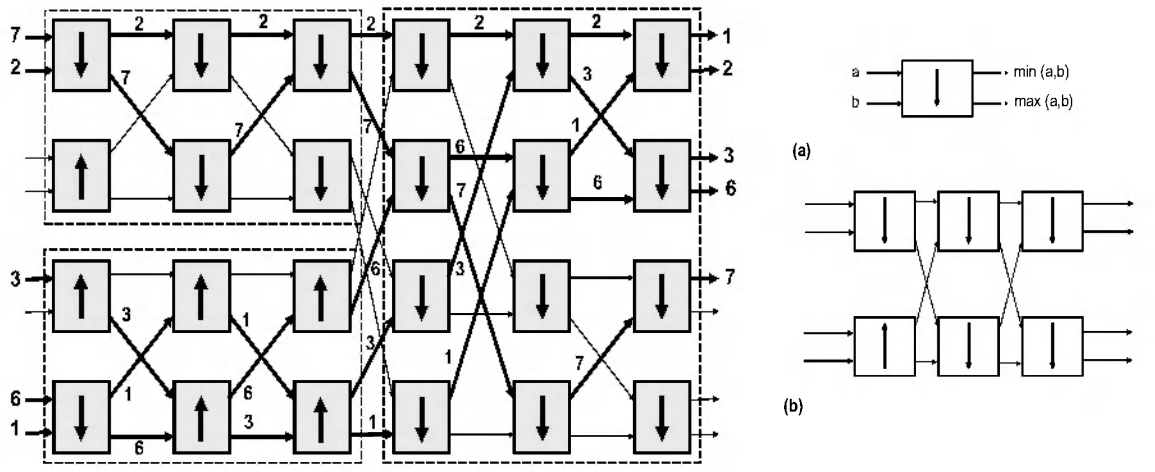

Fig. 2.- Example of routing in an 8 x 8 Batcher network. (a) Basic comparison block and definition. (b) 4 x 4 Batcher switch.

A way to solve this problem is to locate previously a Batcher sorting network. The basic definition to construct it appears in Fig 2. The Batcher network can sort input packets according to their output port addresses in an ascending order. A comparison block compares the inputs coming to its two input ports. According to arrow sense, the input with a maximum value appears at the output where the arrow indicates. Minimum value goes out through the other output. An 8 x 8 Batcher appears in Fig. 3. An example of routing five signals appears in this figure. In its first stage two half-size Batcher networks sort inputs into two monotonic subsequences: one increasing and one decreasing. The second stage then merges the two subsequences into one single ascending sequence. According to the merging algorithm by Batcher[2], corresponding elements in the two subsequences are formed into pairs and compared. Those that are larger are grouped into one new subsequence, and

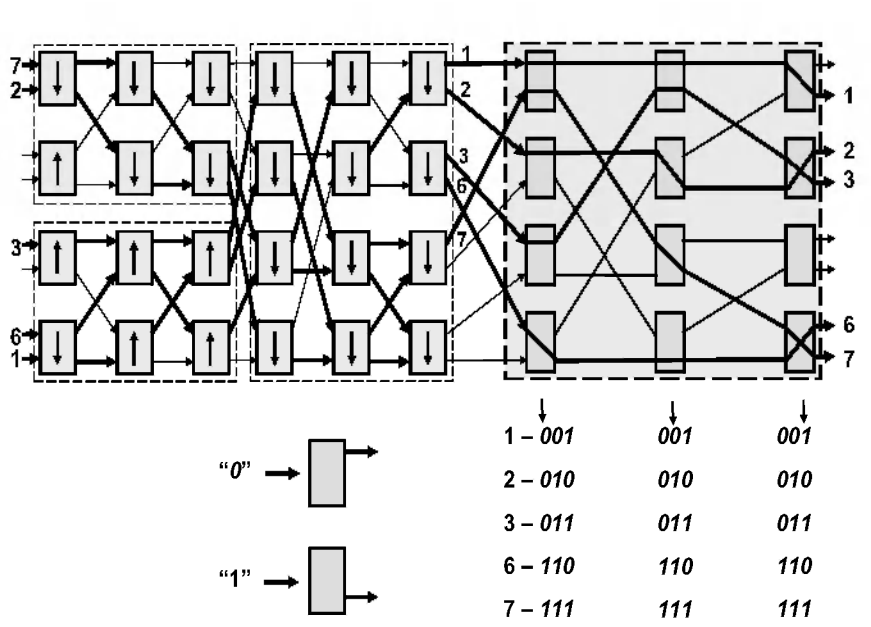

Fig. 3.- An 8 x 8 Batcher – Banyan structure and a possible signal routing.

those that are smaller are grouped into another. Each of two subsequences is then split into half for similar comparisons. This process repeats until each of the final subsequences has only one element. The final outcome is a sorted sequence. The result to combine a sorting network and a self-routing network is a configuration with zero internal blocking. The network of Fig. 3 is an example and it will be the structure to be adopted by us.

3. BASIC UNIT TO CONSTRUCT PHOTONIC SWITCHING ARCHITECTURES: OPTICALLY PROGRAMMABLE LOGIC CELL, OPLC

The basic unit to be employed by us to construct photonic switching architectures is a Logic Programmable Cell employed previously by us as a part of a possible optical computer[3-5]. Although this structure has been reported in several places, some of its principal characteristics will be here presented again. Its main characteristic is the logic processing of two input binary signals, governed by two control signals. Two outputs give logical functions of these inputs. The type of processing is related to the eight main Boolean Functions, namely, AND, OR, XOR, NAND, NOR, XNOR, ON and OFF. The programmable ability of the two outputs, as it has been described, will allow the generation of several data coding for optical transmission. Moreover, as it will be shown too, this circuit has the possibility to the generation of periodic and even chaotic solutions. A precise analysis of the output characteristic versus the main variable parameters, as control signal level and data signal level, has been reported[3-4].

With this configuration, the above-mentioned digital character of the signal is directly obtained. Its main blocks are shown in Fig. 4. Two devices with a non-linear behaviour, P and Q, compose the circuit. The outputs of each one of them correspond to the two final outputs, O_1 and O_2, of the cell. Four are the possible inputs to the circuit. Two of them are for input data, $\mathbf{I_1}$ e $\mathbf{I_2}$, and the other two, ***g*** and ***h***, for control signals. The way these four inputs are arranged inside the circuit is also represented in Figure 4. A practical implementation we have carried out of the processing element has been based on an optoelectronic configuration. Lines in Fig. 4 represent optical fibres. The indicated blocks, placed in order to combine the corresponding signals, are conventional optical couplers. In this way, optical inputs arriving to the individual devices are multilevel signals. The characteristics of the non-linear devices are also shown in Fig. 4. Device Q, corresponds to a thresholding or switching device, and device P is a multistate device, being the response of this non-linear optical device the one represented in the inbox of Fig. 4. This response is similar to the behaviour of a SEED (Self-Electrooptical Effect Device).

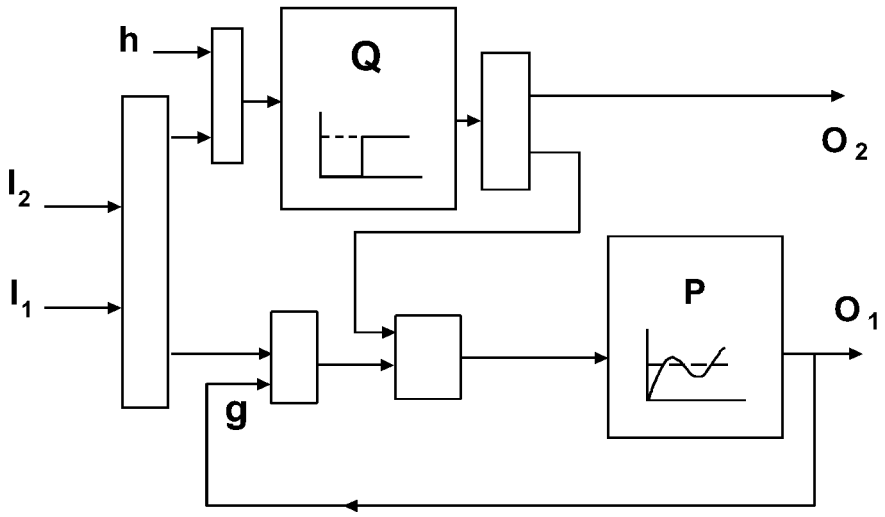

Fig. 4.- Optically Programmable Logic Cell main blocks

A possibility given by our OPLC is to obtain an optical generator with a frequency variable able to be applied to different uses. The solution to be adopted is to introduce a feedback between an output gate of the OPLC and one of the possible inputs. In our present case we have taken the output corresponding to the P device. This feedback introduces, as it can be seen in Fig. 4, a time delay. This time delay determines the frequency of the oscillation. Moreover, it is necessary to introduce an input signal. In the present case, this signal is a continuous obtained from a step function. It is important to recall that the oscillation frequency is a function of the introduced time delay. This time delay has been designed in such a way that the signal need to set up its

configuration, determines the delay and, as a consequence, the frequency. In some way, it works as a VCO (Voltage Controlled Oscillator). The implemented system appears in Fig. 5 where the main blocks are present. Fig. 6 gives an example of its computer simulation. In the present situation, three are the values given to the control signal determining the value of three time delays at the feedback.

4. BASIC CONFIGURATION OF THE PROPOSED SYSTEM

In order to construct a switching structure able to route optical packets, a Batcher-Banyan architecture can be arranged with OPLCs as basic units. The general structure is the same one shown in a previous paragraph. We will restrict here to the main points related with the behavior of OPLCs when this application is intended.

The first step will be to determine the method to obtain the behavior indicated in Fig. 2.a. The principal aspect to consider is designing the way an input bit "1" always appears at the output port indicated by the arrow whereas a bit

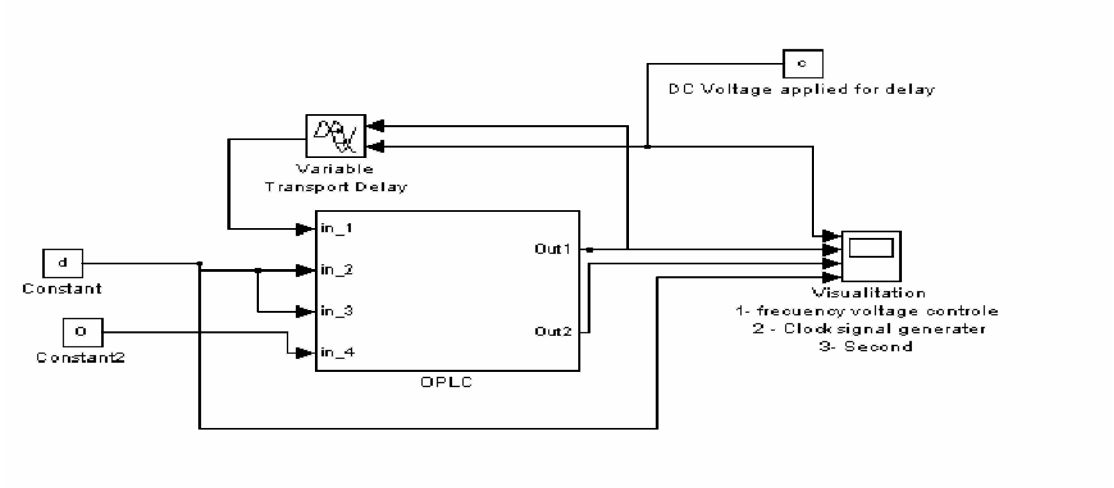

Fig. 5.- Basic configuration of the optical generator for the auxiliary signal.

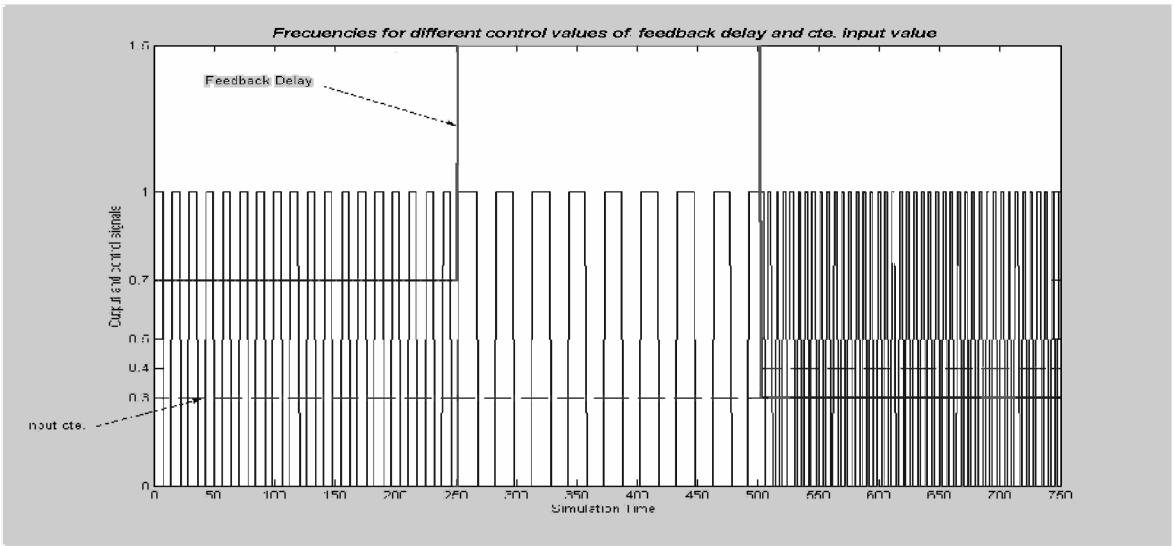

Fig. 6. - Periodic solutions obtained for three different feedback times in Fig. 5.

"0" goes out through the other port. There is no difference with respect to the inputs for "1" and "0" bits: any one of the two inputs may receive any one of them. Moreover, if two "0"s or two "1"s go to input gates, output gates give the same signals. These results indicate that the operation performed inside the cell is an OR. Some other logic operations may give similar results but just this one will be considered here.

4.1. Basic elements

To perform above indicated operation in the cell, and according to the results reported in previous papers by us [3-5], it is necessary to control the behavior of the cell by a particular signal in the control gate (Fig. 4). As we have indicated previously, this situation corresponds to apply a certain signal over the needed level. This level has to come from the initial bit in the packet. Moreover, this bit has to maintain the same logic function in the OPLC during the time the remaining of the packet last.

The way to achieve the above result is by a bistable laser diode[6]. This bistable laser operates as an optical flip-flop which can be set and reset by optical signals. These signals correspond to the initial bit of the packet. Fig. 7 shows its hysteresis characteristics as the relation among an optical input power P_{in}, output power P_{out}, and injection current I_{i1}. This bistable laser diode can operate as an optical memory by two different methods. Fig. 7.a corresponds to a situation where an injection current I_{i1} is set smaller than threshold current I_2. The laser reaches beyond a P_1 threshold power and laser oscillation stops when optical input power Pin decreases below a P_2 threshold power. Therefore, the bistable laser diode has two stable states E and G and can retain binary optical information as long as bias input power is remaining on P_b. In the indicated in Fig. 7.b the bistable laser begins oscillation without providing optical input power, when injection current I_{i1} reaches beyond an I_1 threshold current. Laser oscillation stops when injection current I_{i1} decreases below an I_2 threshold current. This structure and these behaviors allow us to perform the desired function.

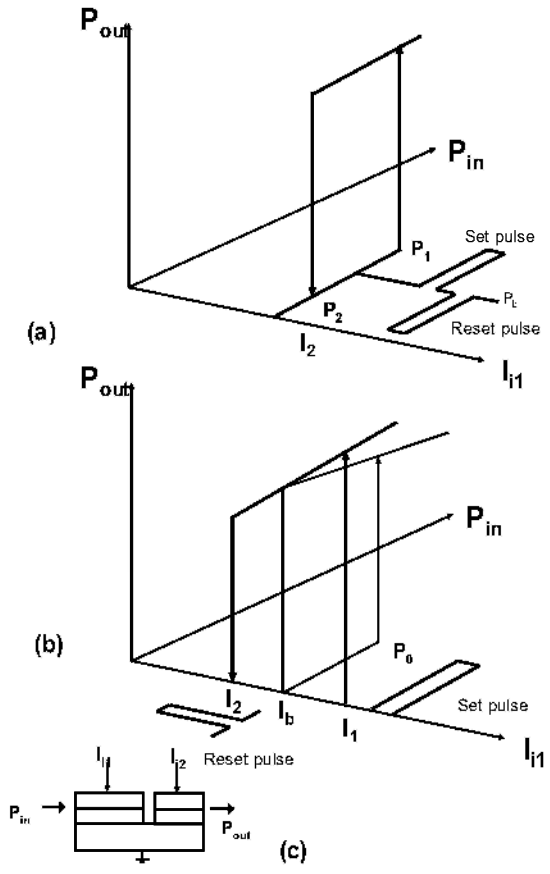

Fig. 7.- (a) (b) Bistable laser diode characteristics (c) Laser diode structure.

4.2. Switching fundamental aspects

The main fundamental point to be addressed in this work is the way to switch packets according to the bits located at certain positions. A general scheme of the operation appears in Fig. 8. The principal steps to be considered are indicated there.

The OPLC reported previously has to act as a switching element able to route a packet to one of its two possible outputs. The main problems to be addressed are the followings:

a. The bit corresponding to a certain position indicates the output where the whole packet has to be routed.
b. A bit "1" indicates that the packet will appear at the upper output.
c. A bit "0" indicates that the packet will appear at the lower output.
d. The whole packet has to go out through the same output port.
e. No signal has to appear at the second output port.
f. If two signals collide in the same port they should have different optical frequencies.

A first consequence of these facts is the need to maintain the OPLC at the same logic state during the interval used by a packet. The second consequence is the need to recognize the bit located at a certain position and indicating the output to be addressed. The total processes to achieve these facts appear in Figs. 9-14.

The first step will be to generate pulses corresponding to the different columns. Three bits will be the needed in the case of the Banyan shown in Fig. 3. These bits are achieved with a simple structure as the one shown in Fig. 9. A periodic train of pulses, obtained with the configuration appearing in Fig. 5, arrives to one of the two possible inputs of three OPLCs. This train of pulses has the same frequency of the input information signal. Another pulse is generated from an auxiliary generator. This pulse arrives at remaining port of the first OPLC at the same time than the first pulse of the auxiliary periodic train. If the function adopted for the cell is an AND, the result will be just a pulse at the position of the first bit. Delay lines impose additional times to similar pulses for second and third OPLCs. The resulting signals will be pulses located at the successive positions of the signal bits. This operation may be achieved in a simple way, just by a simple initial pulse, division in the number of necessary pulses and successive delays. But this structure allows obtaining pulses with the characteristics needed for different situations, namely, optical frequency, time length and shape.

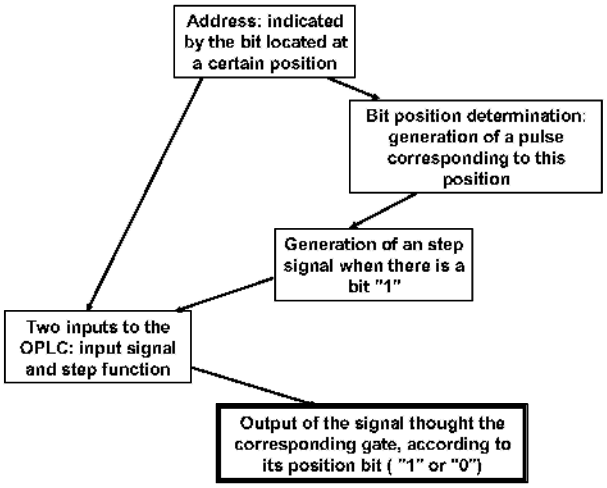

Fig. 8.- Main blocks for the system.

Next phase is obtaining the step functions needed to maintain the OPLCs open for the rest of the packet. The adopted solution appears in Fig. 10. Two are possible cases represented. Information signal enter to the OPLC through one of the gates. A pulse corresponding to the address to be read enters through the other one. The two represented cases show the two possible situations: bit "1" and bit "0". One of the outputs, the lower one, gives the AND function of the input signals. When there are two bits "1" at the same position, a bit "1" will appear at this output. If the information signal has a "0" at this position, there will be "0" output. The second output, represented too in the figure, is used for other functions. The resulting signal, a bit "1" or a "0" enters to a bistable laser diode as the one shown in Fig. 7. The resulting signal will be a step function in the case of a bit "1" and no function in the case of a bit "0".

Next step corresponds to the switching functions. As I was pointed out before, the initial bit, corresponding to the packet to be addressed, brings the laser to the upper state and its signal goes to one of the control gates of the OPLC. This signal, as it may be seen in the working diagram of the OPLC, brings it to the state where an OR function is performed. With this function, the output through upper gate will be the remaining bits in the packet. On the contrary, if initial pulse in the packet is a "0", output will go through the lower gate. A simple scheme of this configuration appears in Fig. 11. Two possible cases are indicated. Packet A has a bit "1" as first digit. Packet B has a "0". This bit, going through a bistable laser diode, sends the corresponding order to one of the OPLC control gates. The following bits in the packet,

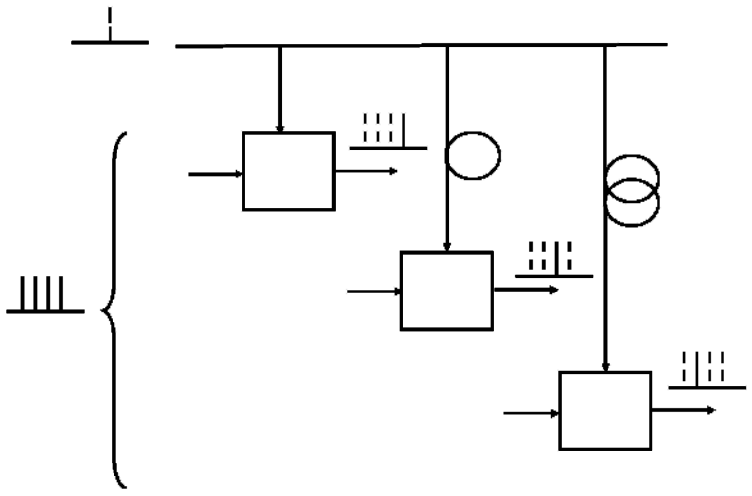

Fig. 9.- Generation of pulses corresponding to each one of the address positions.

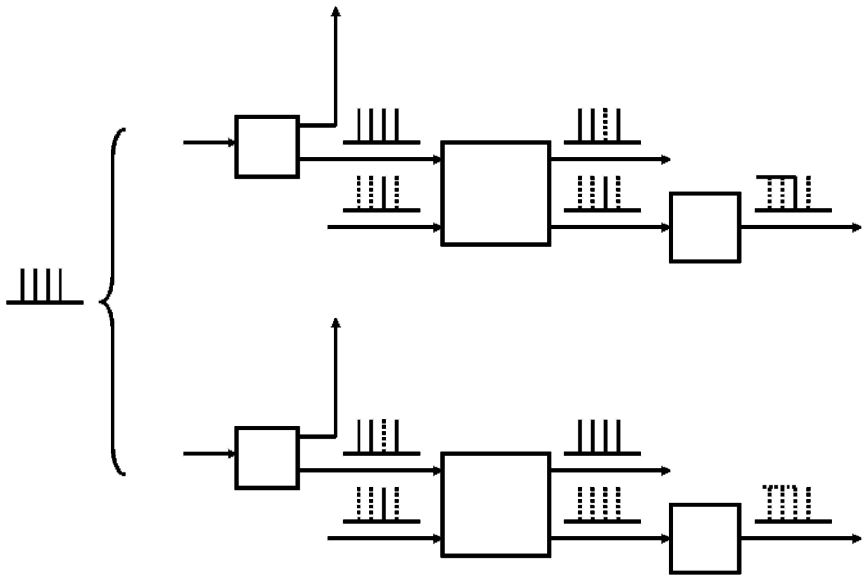

Fig. 10.- Generation of step signals according to the address bit: "1" generates step signal, "0" does not generates step signal.

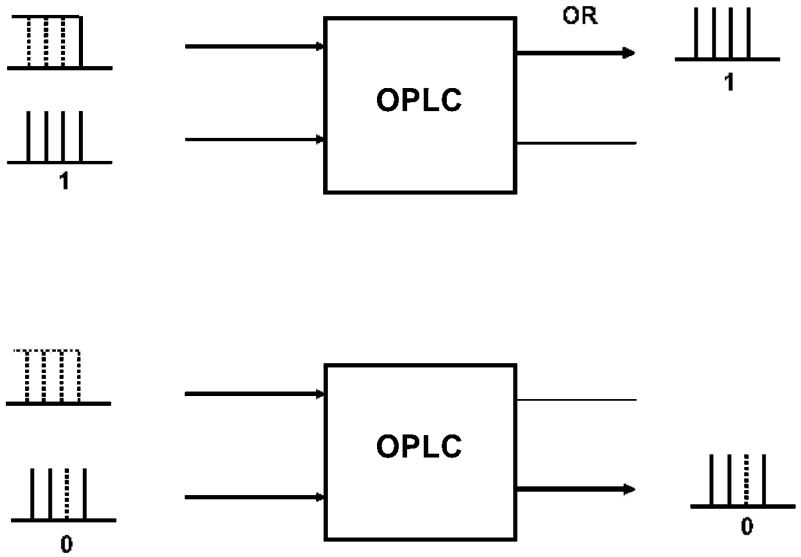

Fig. 11.- OPLC outputs corresponding to different addresses.

because the bistable characteristics of the laser, go through the path determined by this first bit. Bistability allows maintaining the same situation during the packet time. After this time, laser diode goes back to the first state, under threshold. Next packet will repeat the same operation.

An advantage of this configuration is that a more versatile behavior may be allowed. As it was pointed out before, if through the second gate of the OPLC goes another signal with an address whose initial bit is a "1" too, blocking appears. In the present situations, and according to Fig. 6, two different signals may go through the same path when their wavelengths are different. A possible solution is to convert it before going into the OPLC by a wavelength converter, for instance, a SOA. This allows both signals go through similar paths and have a similar behavior.

These ideas have been implemented by computer simulation and the general scheme to switch a signal according to its first two bits appears in Fig. 12. Extensions to higher order switching may be done in a very straightforward way. As it can be seen, two are the inputs to the system: a sequence of reading pulses, located at the position to be detected in each packet, and a data stream corresponding to the signal to be routed. Each one of the blocks corresponds with an OPLC being its particular inputs and outputs, as well as its

control signal and external connections, the ones indicated in Fig. 13. In Fig. 13, the main block corresponds to an OPLC as the one shown in Fig. 4.

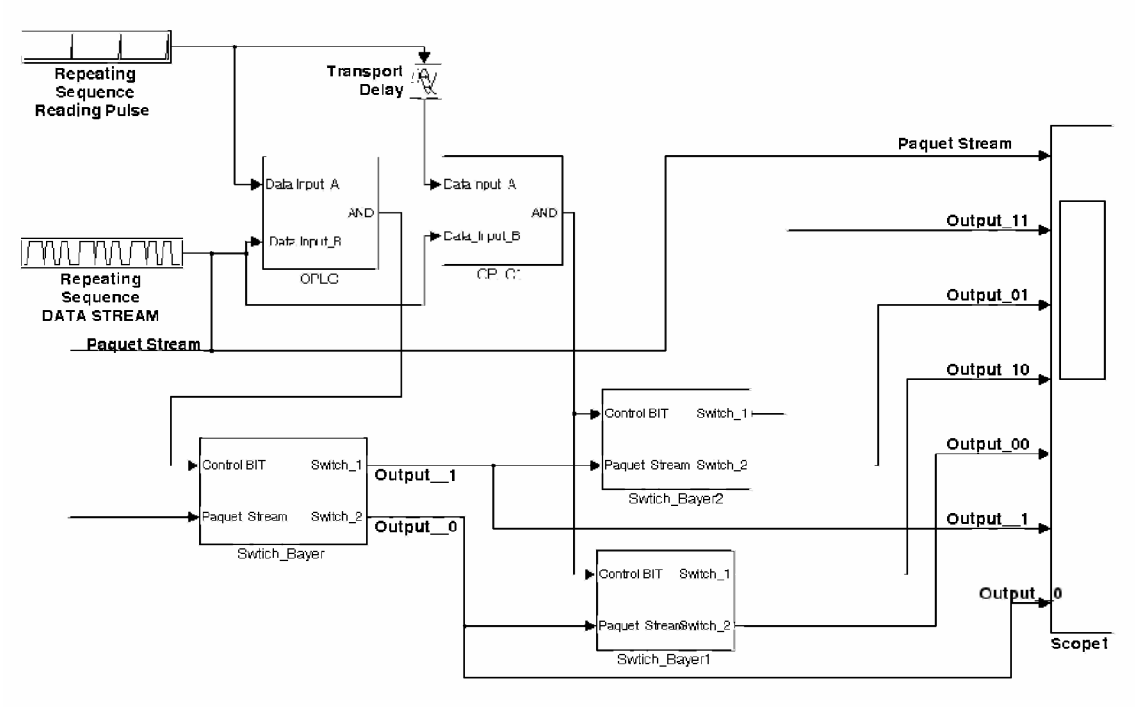

Fig. 12.- General scheme of the computer simulation for the proposed system.

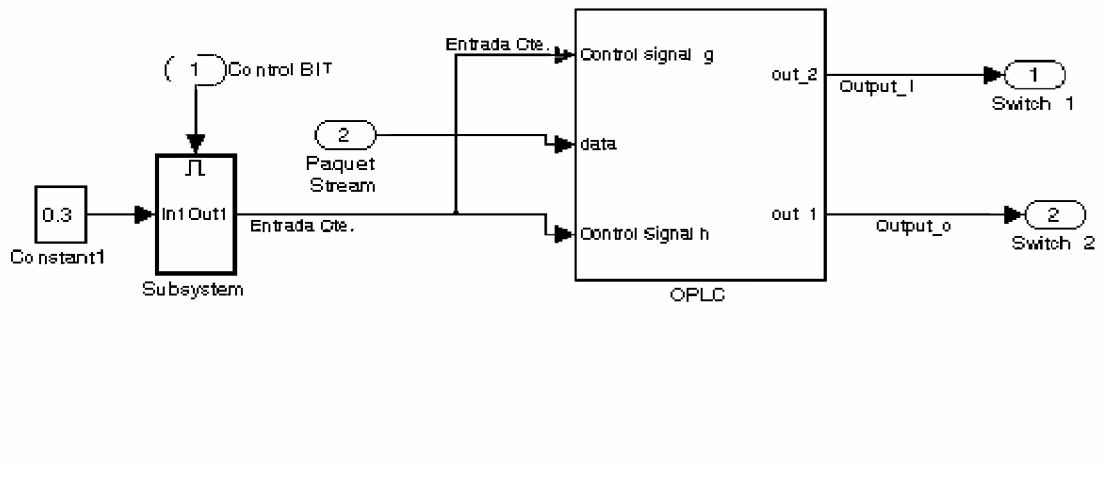

Fig. 13.- Internal configuration of the blocks in Fig. 12. Black box corresponds to an OPLC (Fig. 4).

An example of the functioning of this system appears in Fig. 14. Two address bits route the packet to the corresponding gate according to their information.

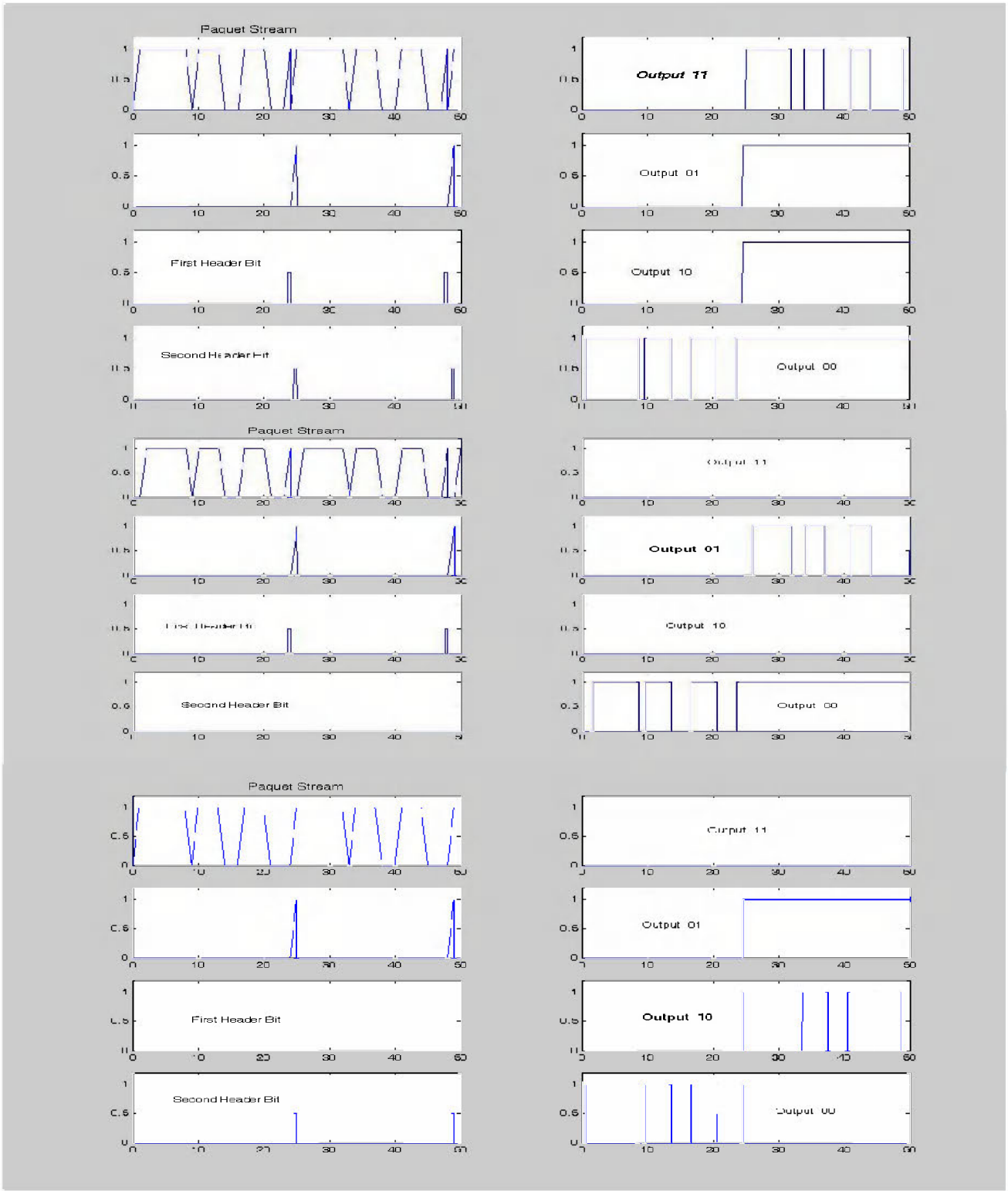

Fig. 14.- Results obtained from the computer simulation.(Figs. 12-13) for switching corresponding to the first two address bits.

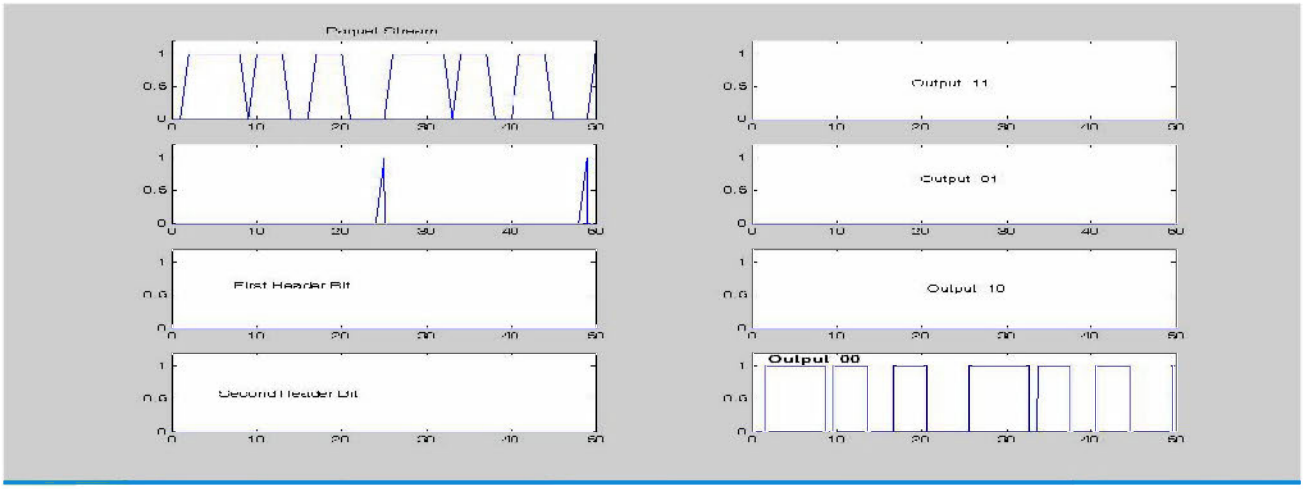

Fig. 14 (con.)

5. CONCLUSIONS

The work reported in this paper is just a simple presentation of some of the possibilities obtained when devices employed in Optical Computing are used in Optical Communications. The reported application in photonic switching shows a possible way to implement communication systems by optical logic elements. The main advantage of this new method is the possibility to handle both signals with packets format and signals with different optical frequency. This possibility comes from the different behavior had by nonlinear optical components with the wavelength. A simple case with two address bits has been reported but extension to higher orders may be implemented. Moreover, some other configurations may be implemented when the concepts employed in optical switching should be introduced in add-drops, as it was shown previously by us[7].

ACKNOWLEDGMENTS

This work was partly supported by CICYT "Comisión Interministerial de Ciencia y Tecnologia", grant TIC99-1131 and CAM "Comunidad Autónoma de Madrid", grant 07T/0037/2000.

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